PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Risho KOH, et al.

Docket No: Q76865

Appln. No.: Unknown

Confirmation No.: Unknown

Group Art Unit: Unknown

Filed: September 24, 2003

Examiner: Unknown

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

1. U.S. Patent Application Publication No. 2002/0185687 A1, published December 12, 2002. **This application is related to the above-referenced case.**

2. JP-A 4-34980 published February 5, 1992, to Mitsubishi Electric Corp., with English Abstract.

3. KOH et al., "Body-Contacted SOI MOSFET Structure with Fully Bulk CMOS Compatible Layout and Process", *IEEE Electron Device Letters*, Vol. 18, No. 3, March 1997, pp. 102-104.

4. CHEN et al., "Suppression of the SOI Floating-body Effects by Linked-body Device Structure", *1996 Symposium on VLSI Technology Digest of Technical Papers*, June 11-13, 1996, pp. 92-93.

5. JP-A 2000-294794 published October 20, 2000, to Hitachi, Ltd., with English Abstract.

6. MAEDA et al., "Impact of 0.18μm SOI CMOS Technology using Hybrid Trench Isolation with High Resistivity Substrate on Embedded RF/Analog Applications", *2000 Symposium on VLSI Technology Digest of Technical Papers*, June 13-15, 2000, pp. 154-155.

7. JP-A 2002-217420 published August 2, 2002, to Samsung Electronics Co., Ltd., with English Abstract.

8. YAMAGAMI et al., "Thin Film SOI-MOSFET with Body Contact Structure using Elevated Field Insulator", *The Japan Society of Applied Physics, The 63rd Autumn Meeting, 2002*, September 24, 2002, pp. 801, with English translation.

9. JP-A 11-135795 published May 21, 1999, to NEC Corp., with English Abstract.

10. JP-A 2001-24202 published January 26, 2001, to Hyundai Electronics Ind. Co., Ltd., with English Abstract.

11. WO 03/023865 A1 published March 20, 2003, to NEC Corp., with English Abstract.

12. JP-A 2000-332250 published November 30, 2000, to Sony Corp., with English Abstract.

13. JP-A 2000-252471 published September 14, 2000, to NEC Corp., with English Abstract.

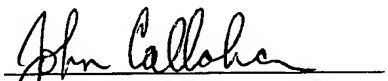
One copy of each of the listed documents, other than any U.S. patents and patent publications, is submitted herewith.

The present Information Disclosure Statement is being filed: (1) No later than three months from the application's filing date for an application other than a continued prosecution application (CPA) under §1.53(d); (2) Before the mailing date of the first Office Action on the merits (whichever is later); or (3) Before the mailing date of the first Office Action after filing a request for continued examination (RCE) under §1.114, and therefore, no Statement under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,



John T. Callahan
Registration No. 32,607
for J. Frank Osha
Registration No. 24,625

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: September 24, 2003

(7)

Information Disclosure Statement

The present invention is presented in The Japan Society of Applied Physics, The 63rd Autumn Meeting, 2002. The translation of the abstract published on **September 24, 2002** is as follows.

Thin Film SOI-MOSFET with Body Contact Structure using Elevated Field Insulator

S. Yamagami, R. Koh, H. Wakabayashi, J.-W. Lee, Y. Saito, A. Ogura, M. Narihiro, K. Arai, H. Takemura, T. Yamamoto, Y. Ochiai, and T. Mogami

1. Introduction With the progress of miniaturization of semiconductor devices, an SOI layer of an SOI-MOSFET is becoming thinner and thinner. Reducing the thickness of the SOI layer is effective not only in making a high-efficiency full-depletion SOI MOSFET but also in reducing junction capacitance between a source/drain region and a body region in a partial-depletion (PD) SOI MOSFET. There is a problem of floating body effects in the PD SOI MOSFET. A body contact structure is effective in suppressing the floating body effects. However, no body contact structure has been reported so far which is applicable to a thin SOI layer. We developed a body contact structure applicable to a thin SOI layer by using a device isolating structure elevated over the thin SOI film (Fig. 1). The body contact structure is also applicable to a bulk substrate.

2. Methods First, channel ion is implanted in the SOI layer of 30 nm thick, and a gate oxide/nitride film is formed. Next, a first gate polysilicon film and a nitride film as a mask in a CMP process are formed. Then, the nitride film and the first gate polysilicon film in a device isolating region are removed by a dry etching. The SOI layer therein is not removed, which is to be a path contacting a body region. Impurity is

heavily introduced into this SOI layer in order to evacuate lots of carriers in the body region. After that, a device isolating oxide film is formed, a CMP is carried out by using the nitride film as a mask, and then the nitride film is removed. In this way, the device isolating structure is attained, in which a field insulating film is elevated over the SOI layer. After forming a second gate polysilicon film, the transistor device is formed by a normal MOS process.

3. Results Figs 2 and 3 show I_D-V_D characteristics of an SOI-pMOSFET with the body contact structure using the elevated field insulator and a normal SOI-pMOSFET, respectively (Lg = 80 nm). In the case of the normal SOI pMOSFET without a body contact structure, a kink appears due to the floating body effects. On the other hand, no kink appears in the case of the SOI-pMOSFET with the body contact structure using the elevated field insulator. Therefore, the present body contact structure is effective in suppressing the floating body effects, even in the case of such a thin SOI film of 30 nm.

Substitute for Form 1449 A & B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	Unknown
Confirmation Number	Unknown
Filing Date	September 24, 2003
First Named Inventor	Risho KOH
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	Q76865

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number	Document Number: Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US 2002/0185687	A1	12-12-2002	NEC Corporation
		US			
		US			
		US			
		US			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]	Foreign Patent Document: Number[4]	Foreign Patent Document: Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation[6]
		JP	4-34980	A	02-05-1992	Mitsubishi Electric Corp.	Abstract
		JP	2000-294794	A	10-20-2000	Hitachi Ltd.	Abstract
		JP	2002-217420	A	08-02-2002	Samsung Electronics Co., Ltd.	Abstract
		JP	11-135795	A	05-21-1999	NEC Corp.	Abstract
		JP	2001-024202	A	01-26-2001	Hyundai Electronics Ind. Co., Ltd.	Abstract
		WO	03/023865	A1	03-20-2003	NEC Corp.	Abstract
		JP	2000-332250	A	11-30-2000	Sony Corp.	Abstract
		JP	2000-252471	A	09-14-2000	NEC Corp.	Abstract

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation[6]
		KOH et al., "Body-Contacted SOI MOSFET Structure with Fully Bulk CMOS Compatible Layout and Process", *IEEE Electron Device Letters*, Vol. 18, No. 3, March 1997, pp. 102-104	
		CHEN et al., "Suppression of the SOI Floating-body Effects by Linked-body Device Structure", *1996 Symposium on VLSI Technology Digest of Technical Papers*, June 11-13, 1996, pp. 92-93	
		MAEDA et al., "Impact of 0.18μm SOI CMOS Technology using Hybrid Trench Isolation with High Resistivity Substrate on Embedded RF/Analog Applications", *2000 Symposium on VLSI Technology Digest of Technical Papers*, June 13-15, 2000, pp. 154-155	
		YAMAGAMI et al., "Thin Film SOI-MOSFET with Body Contact Structure using Elevated Field Insulator", *The Japan Society of Applied Physics, The 63rd Autumn Meeting, 2002*, September 24, 2002, pp. 801, with English translation	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kind Codes of USPTO Patent Documents at www.uspto.gov, MPEP 901.04 or in the comment box of this document. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to indicate here if English language Translation is attached.